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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/843,649	04/27/2001	Kenji Morita	Q64244	7847

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EXAMINER	
PHAM, THIERRY L	

ART UNIT	PAPER NUMBER
2624	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/843,649	MORITA ET AL.	
	Examiner	Art Unit	
	Thierry L. Pham	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/18/02

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

- This action is responsive to the following communication: an Amendment filed on 11/9/05.
- Claims 1-3, and 5; claim 4 has been canceled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Kamada et al (US 6388675).

Regarding claim 1, Kamada discloses an image processing device (***image processing apparatus, fig. 4, col. 3, lines 59-61***), comprised of a first storage device (***memory 3, fig. 4***), which stores n-bit image data (***8-bits picture data "PIC1", fig. 4, col. 3, lines 65-67***),

- an image data converter (***CPU 1, fig. 1***), which converts said n-bit image data into m-bit (***CPU 1 transfers color palette (8 bits) data from memory 3 to color palette storage 13 (24 bits***) by means of comparison/collation of registered palette address with color palette values, col. 4, lines 10-24) (where n<m) image data, and (***inherently, 24 bits is greater than 8 bits, for example, picture data contains 8 bits image data and 24 bits of color palette values and 24 bits of color palette is transferred to color palette storage section, which further transmitted to a display device, figs. 4-7***)
- a second storage device (***color palette storage/control block 13 for storing data transferred from memory 3, fig. 4, col. 4, lines 10-23***), which stores said m-bit image data resulting from data conversion,
- a transfer controller which controls data transfer, wherein said first storage device (***memory 3 stores both picture data [8 bits] and color palettes [24 bits], fig. 4 and col. 3, lines 65 to col. 4, lines 6 and col. 4, lines 40-42, also see figs. 5a-5b for 24 RBG bits***) stores m-bit color pallet

data corresponding to said n-bit image data, said transfer controller transfers both of said n-bit image data and m-bit color pallet data ***(both image data and color pallet are transferred from memory 3 to graphic display controller 2, fig. 4, col. 4, lines 10-42)*** corresponding to said n-bit image data to said image data converter, and said image data converter converts (***CPU 1 transfers color palette data from memory 3 to color palette storage 13 by means of comparison/collation of registered palette address with color palette values, col. 4, lines 10-24***) said n-bit image data into m-bit image data by collation of said n-bit image data with said m-bit color pallet data and then transfers said m-bit image data to said second storage device (color palette storage/control block 13 for storing data transferred from memory 3, fig. 4, col. 4, lines 10-23). ***Please note: According to the original filed specification, the method for converting n-bits to m-bits involves collating the index value of image data (i.e. 8 bits) with color palette values (i.e. 16 bits) and transfers the color palette values (16 bits) to a second storage area, please see figs. 7 & 10 for "conversion process". Kamada explicitly discloses the same method for converting picture data (i.e. picture data contains 8 bits image data and 24 bits of color palette values) and 24 bits of color palette is transferred to color palette storage section, which further transmitted to a display device, figs. 4-7.***

Regarding claim 2, Kamada discloses an image processing device as claimed in claim 1, (image processing apparatus, fig. 4, col. 3, lines 59-61) further comprising:

- a display device (display 4, fig. 4), which displays, as image information, said m-bit image data read out from said second storage device (display color palette values, which represents higher bits than picture data, col. 4, lines 56-58), wherein said image data converter converts (CPU 1 transfers color palette data from memory 13 to color palette storage 13 by means of comparison/collation of registered palette address with color palette values, col. 4, lines 10-24) said n-bit image data, stored in said first storage device, into m-bit image data for each pixel (fig. 5a-5b) that comprises said image information that is to be displayed on said display device (display device 4, fig. 4) and then transfers said m-bit image data to said second storage device.

Regarding claim 3, Kamada further discloses an image processing device as set forth in claim 1, wherein said image data converter successively acquires (i.e. successively scans and

converts picture area via corresponding by palette number, fig. 7c) said n-bit image data for single image information that have been transferred from said first storage device and the m-bit (where n<m) color pallet data corresponding to the image data and acquires said color pallet data for each pixel (i.e. one dot, col. 6, lines 10-11) that forms said single image information and then transfers converted m-bit imaged data to said second storage device (CPU 1 transfers color palette data from memory 13 to color palette storage 13 by means of comparison/collation of registered palette address with color palette values, col. 4, lines 10-24).

Regarding claim 5, Kamada discloses an image data conversion method, with which n-bit image data (8-bits picture data "PIC1", fig. 4, col. 3, lines 65-67) stored in a first storage device (memory 3, fig. 4) and m-bit (where n<m) color pallet data (24 bits color palette data, fig. 4), which correspond to the image data and are stored in the first storage device, are used to perform conversion, comprising:

- acquiring said n-bit image data (8 bit picture data, fig. 4, col. 3, lines 65-67) and said m-bit color pallet data (***memory 3 stores both picture data [8 bits] and color palettes [24 bits], fig. 4 and col. 3, lines 65 to col. 4, lines 6 and col. 4, lines 40-42, also see figs. 5a-5b for 24 RBG bits***) from said first storage device;
- transferring ***(both image data and color pallet are transferred from memory 3 to graphic display controller 2, fig. 4, col. 4, lines 10-42)*** both of said n-bit image data and n-bit image data and m-bit color pallet data corresponding to said n-bit image data; and
- converting said n-bit image data to m-bit image data by collation of said n-bit image data with said m-bit color pallet data ***(CPU 1 transfers color palette data from memory 13 to color palette storage 13 by means of comparison/collation of registered palette address with color palette values, col. 4, lines 10-24)*** which have been transferred.

Please note: According to the original filed specification, the method for converting n-bits to m-bits involves collating the index value of image data (i.e. 8 bits) with color palette values (i.e. 16 bits) and transfers the color palette values (16 bits) to a second storage area, please see figs. 7 & 10 for "conversion process". Kamada explicitly discloses the same method for converting picture data (i.e. picture data contains 8 bits image data and 24 bits

of color palette values) and 24 bits of color palette is transferred to color palette storage section, which further transmitted to a display device, figs. 4-7.

Response to Arguments

Applicant's arguments filed 11/09/05 have been fully considered but they are not persuasive.

• Regarding claim 1, the applicants argued the cited prior art of record (US 6388675 to Kamada et al) fails to teach and/or suggest storing image data and corresponding color pallet data in a first memory and transferring the image data and the corresponding color pallet data to an image data converter.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., storing image data and corresponding color pallet data in a first memory and transferring the image data and the corresponding color pallet data to an image data converter) are not recited in the previous rejected claim 1. However, Kamada clearly teaches storing image data and corresponding color pallet data in a first memory (memory 3 as shown in fig. 4 stores both image data "PIC 1" and corresponding color palette, col. 4, lines 38-45, and see fig. 7 for more details) and transferring (transferring via cable 5 as shown in fig. 4, col. 4, lines 10-24) the image data and the corresponding color pallet data (transferring both image data and corresponding color palette from memory 3 to graphic display controller 2 as shown in fig. 4, CPU 1 of fig. 4 controls the transmissions of image data and color palette) to an image data converter.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thierry L. Pham whose telephone number is (571) 272-7439. The examiner can normally be reached on M-F (9:30 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David K. Moore can be reached on (571)272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thierry L. Pham

GABRIEL GARCIA
PRIMARY EXAMINER